A LOW NOISE DISTRIBUTED AMPLIFIER WITH GAIN CONTROL*

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ABSTRACT

A 2 to 18GHz monolithic GaAs distributed amplifier has been developed with 17dB nominal gain, less than 2.0:1 input and output VSWR, less than 6.0dB noise figure, and greater than 40dB gain control. The chip size at 3.0 sq. mm. (1.63mm by 1.88mm) makes it cost effective for a wide variety of applications.

INTRODUCTION

The functional density of GaAs MMIC's will continue to grow as new monolithic circuit techniques evolve. Already, GaAs MMIC amplifiers covering 2 to 18GHz and beyond have become virtually commonplace (1,2,3,4) and several researchers have reported results on two stage amplifiers (5,6). The MMIC amplifier described in this paper is a two stage distributed amplifier designed specifically for low noise and gain control. These attributes make it ideal for applications that require high dynamic range, amplitude matching, and/or gain compensation over temperature.

CIRCUIT DESIGN

A photograph of the amplifier is shown in Figure 1 followed by a schematic of a single stage in Figure 2. Note that the amplifier consists of two AC coupled stages in an area of 1.63mm by 1.88mm for a total area of 3.0 sq. mm. Each amplifier stage contains six sections of 150 micron cascode connected FET's for a total gate periphery of 3.6mm per chip.

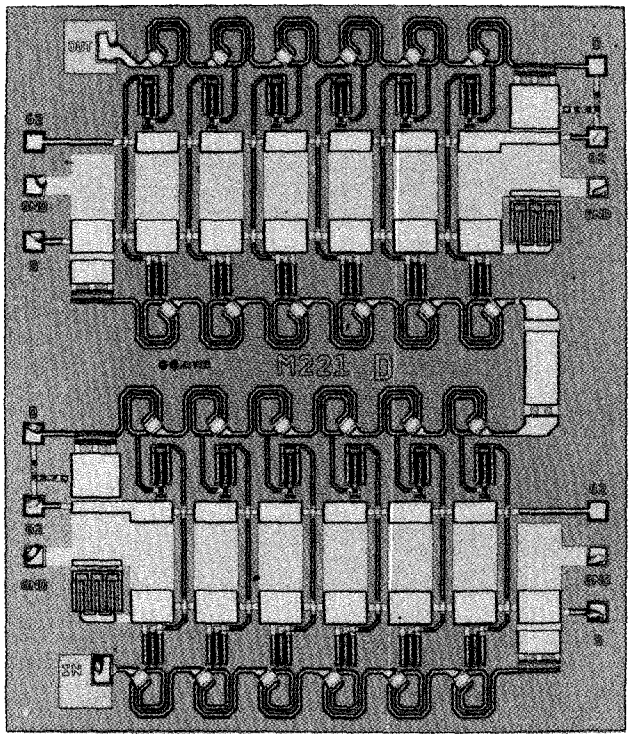

Figure 1. Photograph of the Two-Stage Distributed Amplifier

An on-chip biasing network consisting of a voltage divider for the common gate FET and a source resistor for the common source FET enables the user to operate the amplifier with a single supply (7).

*This program was supported by the Wright Patterson Air Force Base under Contract No. F33675-85-C-1728 and the U.S. Army LABCOM under Contract No. DAAK20-85-Q-0270.

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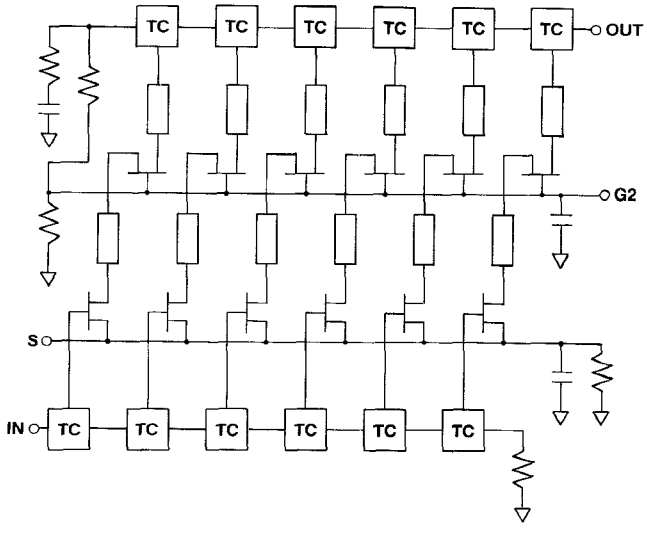

Figure 2. Schematic Diagram of One Stage of the Distributed Amplifier

The cascode FET arrangement (common source FET driving a common gate FET) provides four advangages over a single common source FET as the active element of a distributed amplifier. First, the output impedance of the cascode connected FET is much higher than that of a common source FET. Since the output impedance of the device periodically loads the output transmission line, there is much less attenuation of the output signal and hence higher gain.

Second, the cascode connected FET has much higher reverse isolation than a common source FET. The lower effective feedback capacitance permits greater bandwidth.

Third, the transmission lines between the common source and common gate FET's are very effective in tuning the gain response of the amplifier for optimum gain flatness.

And finally, gain control may be achieved by varying the voltage on the gates of the common gate FET's. This approach is much better than controlling the gain with the gate voltage of the common source FET. Unlike the common source FET, the input impedance of the cascode combination changes very little with gain control. However, the effective transconductance, which controls gain, changes dramatically.

This design also uses Constant-R networks (7) for the input and output artificial transmission lines (TC in Figure 2). As described in the reference, this technique improves bandwidth by approximately 40% over conventional distributed amplifiers using Constant-K networks. In addition, the tight packing of the networks result in very small coils which contribute to the area efficiency of the design.

Predicted gain and noise figure appear in Figure 3. Predicted gain is approximately 18dB for the two stage amplifier while predicted noise figure is less than 5.0dB over the entire 2 to 18GHz range. The amplifier was specifically designed for minimum noise figure by optimizing the number of sections, the gate periphery per section, and the characteristic impedances of the imput and output transmission lines (8). Between 9 and 18GHz, the resulting design achieves an amplifier noise figure which is no more than 1.5dB greater than the minimum device noise figure. This result demonstrates the potential of distributed amplifiers for broadband low noise applications.

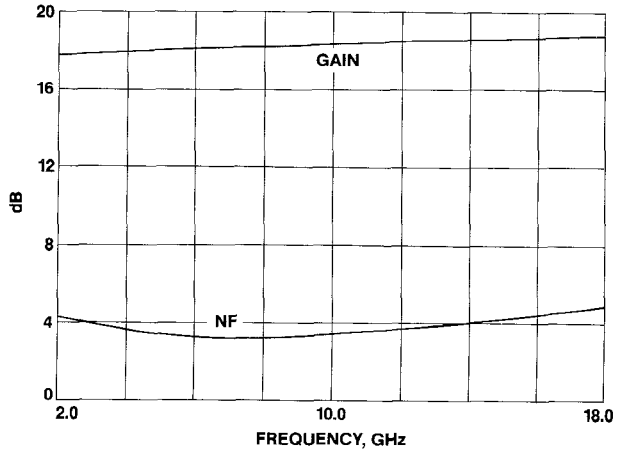

Figure 3. Predicted Gain and Noise Figure of the Two-Stage LNA

CIRCUIT FABRICATION AND PERFORMANCE

Several wafers of this design were fabricated using a standard ion implant process (2). Measured gain, return loss, and noise figure performance are shown in Figures 4 and 5. Power at 1dB compression is displayed in Figure 6. All data presented was measured at 6V and approximately 160mA of current.

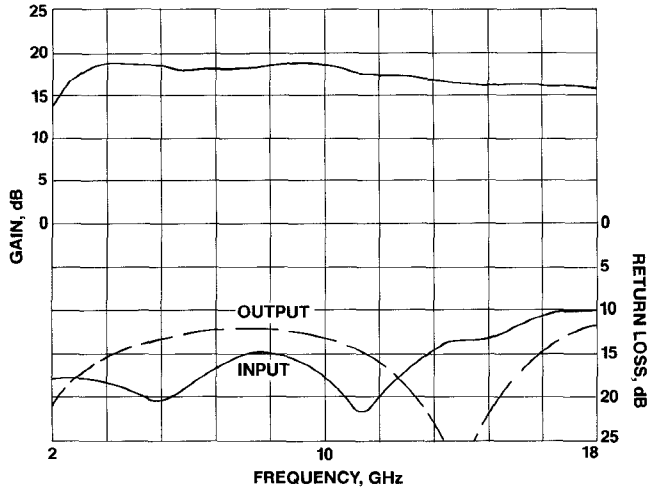

Figure 4. Measured Gain and Return Loss of the Distributed Amplifier

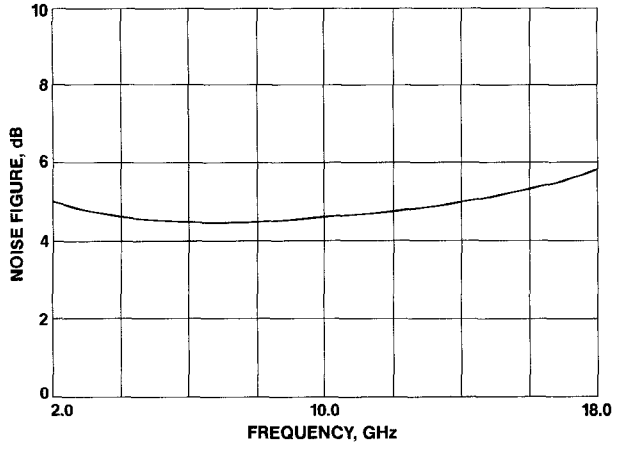

Figure 5. Measured Noise Figure of the Distributed Amplifier

The high frequency rolloff in gain has been traced to high FET gate capacitance and inaccuracies in the model for the Constand-R networks. Nevertheless, the gain response is quite respectable at 17.25dB +/- 1.25dB from 3 to 18GHz. The MMIC chips are mounted on alumina test substrates so data includes all the mounting parasitics.

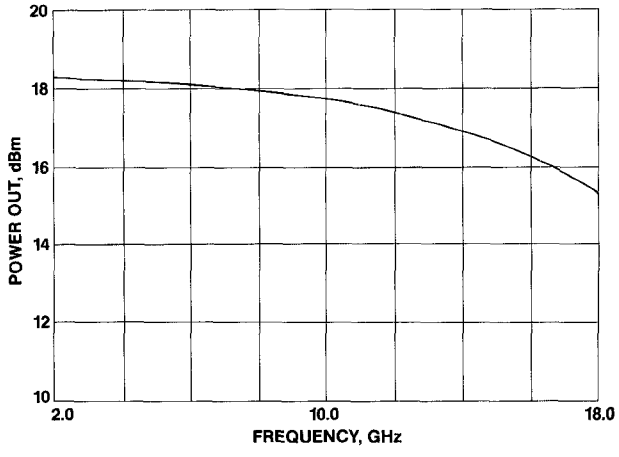

Figure 6. Measured 1dB Compressed Power of the Distributed Amplifier

As mentioned earlier, cascode FET's are ideal for gain control applications. Figures 7, 8, and, 9 demonstrate the gain control capability of the two stage LNA. Figure 7 displays gain as a function of second gate voltage while Figures 8 and 9 show the negligible effect gain control has on both the input and output matches.

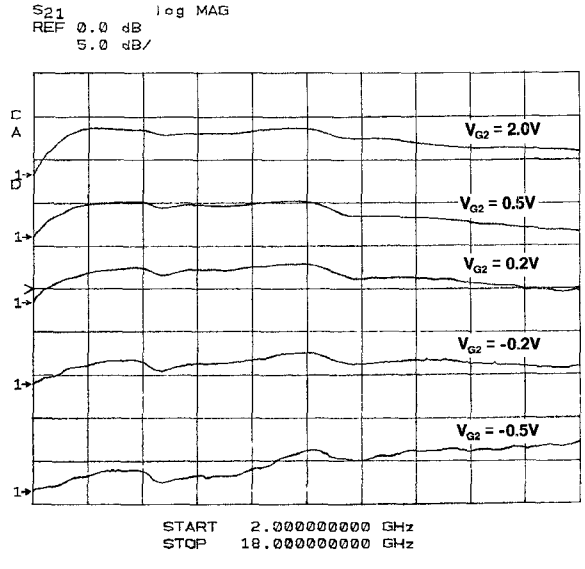

Figure 7. Measured Gain as a Function of G2 Voltage

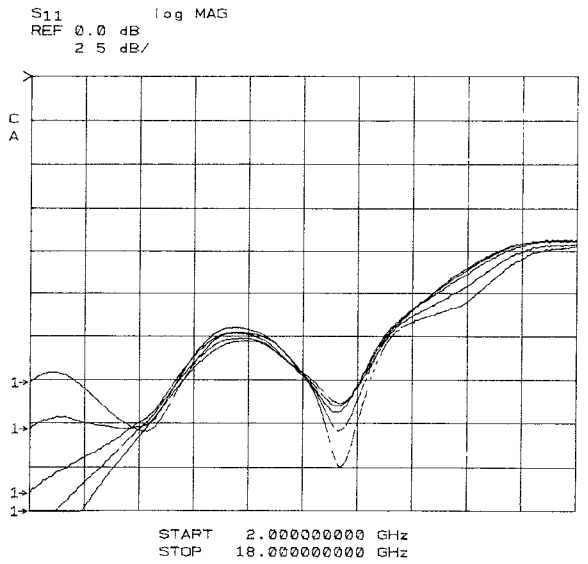

Figure 8. Effect of Gain Control on Input Match

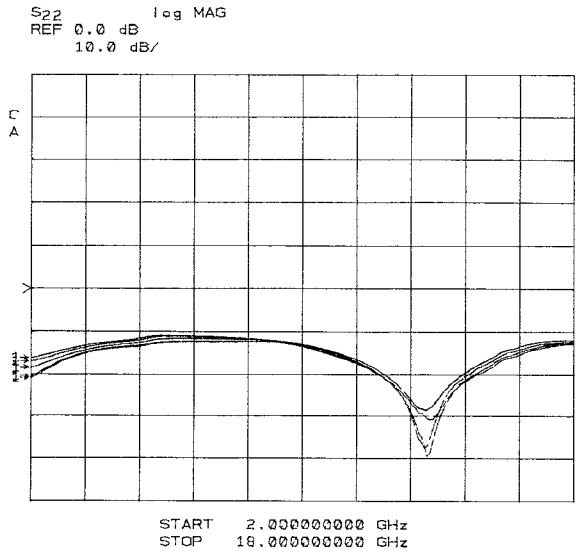

Figure 9. Effect of Gain Control on Output Match

CONCLUSIONS

A two-stage, six-section MMIC distributed amplifier with gain control has been designed and fabricated. Using such techniques as cascode FET's and constant-R networks this amplifier has demonstrated excellent broadband gain, gain flatness, and noise figure. Its performance and compact design make it cost effective for a wide range of applications.

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